What is claimed is:

1. In a multi-threaded processor, a method of assigning thread priority comprising:

determining whether there is an indication of approaching instruction side starvation for a first thread of at least two threads.

2. The method of claim 1 further comprising;

setting a threshold counter to perform a counting operation in response to an indication of approaching instruction side starvation for said first thread.

3. The method of claim 2 further comprising:

resolving instruction starvation after said threshold counter completes its counting operation.

4. The method of claim 3 wherein said resolving instruction starvation comprises:

moving instructions in an execution pipeline of said processor from the second thread to a temporary storage area.

5. In a processor to handle processing of at least first and second threads in parallel, a method of assigning thread priority comprising:

determining if a plurality of conditions for said first thread are true, the conditions including

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

6. The method of claim 5 further comprising:

setting a threshold counter to perform a counting operation if said plurality of instructions are true.

7. The method of claim 6 further comprising:

resolving instruction starvation after said threshold counter completes its counting operation.

8. The method of claim 5 further comprising:

resolving instruction starvation for said first thread by moving instructions in an execution pipeline of said processor from the second thread to a temporary storage area.

9. A multi-threaded processor comprising:

first and second thread queues;

control logic coupled to said first and second thread queues, said control logic to determine if there is an indication of approaching instruction side starvation for a first thread of at least first and second threads.

10. The processor of claim 9 further comprising a threshold counter to perform a counting operation, wherein said control logic is to set said threshold counter if there is an indication of approaching instruction side starvation for said first thread.

11. The processor of claim 10 wherein said control logic is to resolve instruction starvation after said threshold counter completes its counting operation.

12. The processor of claim 11 further comprising an execution pipeline and a temporary storage area wherein said control logic is to move instructions in the execution pipeline of said processor from the second thread to the temporary storage area.

13. A processor to handle processing of at least first and second threads in parallel comprising:

first and second thread queues;

control logic coupled to said first and second thread queues, said control logic to determine if a plurality of conditions are true indicating approaching instruction side starvation for said first thread, the conditions including

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

14. The processor of claim 13 further comprising a threshold counter to perform a counting operation wherein said processor is to set said threshold counter if there is an indication of approaching instruction side starvation for said first thread.

15. The processor of claim 14 wherein said processor is to resolve instruction starvation after said threshold counter completes its counting operation.

16. The processor of claim 15 further comprising an execution pipeline and a temporary storage area wherein said processor is to resolve instruction starvation for said first thread by moving instructions in the execution pipeline of said processor from the second thread to the temporary storage area.

17. A computer system to handle processing of at least first and second threads in parallel comprising:

a memory to store instructions for first and second threads;

a processor coupled to said memory and including

first and second thread queues to store instructions from said first and second threads;

control logic coupled to said first and second thread queues, said control logic to determine if there is an indication of approaching instruction side starvation for said first thread.

18. The computer system of claim 17 wherein said processor further includes a threshold

counter to perform a counting operation, wherein said control logic is to set said threshold counter if there is an indication of approaching instruction side starvation for said first thread.

19. The computer system of claim 18 wherein said control logic is to resolve instruction starvation after said threshold counter completes its counting operation.

20. The computer system of claim 19 wherein said processor further includes an execution pipeline and a temporary storage area wherein said control logic is to move instructions in the execution pipeline of said processor from the second thread to the temporary storage area.

21. A computer system to handle processing of at least first and second threads in parallel comprising:

a memory to store instructions for first and second threads;

a processor coupled to said memory and including

first and second thread queues to store instructions from said first and second threads;

control logic coupled to said first and second thread queues, said control logic to determine if a plurality of conditions are true indicating approaching instruction side starvation for said first thread, the conditions including

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

22. The computer system of claim 21 wherein said processor further includes a threshold counter to perform a counting operation wherein said processor is to set said threshold counter if there is an indication of approaching instruction side starvation for said first thread.

23. The computer system of claim 22 wherein said processor is to resolve instruction starvation after said threshold counter completes its counting operation.

24. The computer system of claim 23 further comprising an execution pipeline and a temporary storage area wherein said processor is to resolve instruction starvation for said first thread by moving instructions in the execution pipeline of said processor from the second thread to the temporary storage area.

25. A set of instructions residing in a storage medium, said set of instructions capable of being executed by a processor to handle processing of at least first and second threads in parallel and assign thread priority comprising:

determining if there is an indication of approaching instruction side starvation for said first thread.

26. The set of instructions of claim 25 wherein the method further includes

setting a threshold counter to perform a counting operation if there is an indication of

approaching instruction side starvation for said first thread.

27. The set of instructions of claim 26 wherein the method further includes

resolving instruction starvation after said threshold counter completes its counting operation.

28. The set of instructions of claim 27 wherein said resolving instruction starvation includes

moving instructions in an execution pipeline of said processor from the second thread to a temporary storage area.

29. The set of instructions of claim 25 wherein determining if there is an indication of approaching instruction side starvation for said first thread includes

determining if a plurality of conditions are true, the conditions including

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

30. The set of instructions of claim 29 wherein the method further includes

resolving instruction starvation for said first thread by moving instructions in an execution pipeline of said processor from the second thread to a temporary storage area.